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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/976,097	10/15/2001	Kazuhiko Nakashita	35.C15883	9347

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EXAMINER

MOE, AUNG SOE

ART UNIT PAPER NUMBER

2685

DATE MAILED: 08/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/976,097	NAKASHITA, KAZUHIKO	
	Examiner	Art Unit	
	Aung S. Moe	2685	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 July 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,4,5 and 9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,4,5 and 9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. The Amendment after Final filed on 7/29/2005 has been entered, however, it does not place the application in condition for allowance because newly discovered reference Yoshida et al of U.S. Pat. No. 6,219, 156 teach the present claimed invention. In view of this, present claimed invention is rejected as follow:

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1, 2, 4, 5 and 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, it is unclear how “an image” recited in lines 5 and 7 related to “an image” recited in line 3? If there are the same “image”, please change “an image” recited in lines 5 and 7 to - - said image - -.

In claim 2, it is unclear how “an image” recited in line 3 related to “an image” recited in lines 3 and/or 5?

In claim 4, it is unclear how “an image” recited in line 3 related to “an image/the image” recited lines 5, 7, and 9 as set forth in Claim 1?

In claim 4, it is unclear how “a readout operation” of reading the image data form the “second area” is parallel with both the “writing operation” and “readout operation” (i.e., noted

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that there is no “readout operation” in claims 1, only “writing operation”), because there is no readout operation prior to “a readout operation” recited in line 2 of claim 4?

In claim 9, it is unclear how “an image” recited in line 6 related to “an image” recited in line 4?

In view of the above, claims 1-2, 4-5 and 9 are given a broadest reasonable interpretation for the purpose of examining.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 5 and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoshida et al. (U.S. 6,219,156).

Regarding claim 1, Yoshida ‘156 discloses an image pickup apparatus (i.e., see Fig. 1; noted the element 91) comprising: an image pickup element (i.e. noted form Figs. 1 and 16, the Image Reader IR contain a sensor, such as CCD sensor, functioned as an image pickup element); a memory (IM) for storing an image obtained by said image pickup element (IR);

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a signal processing circuit (928) adapted to effect predetermined signal processing (i.e., noted from Fig. 3A, the image processing circuit 928 carries out the Compression processing of the image data from the first memory area 9261) on the image read out of a first area (9261) of said memory (IM/926); and

a memory control circuit (i.e., the Fig. 1, the element 927) adapted to, in a mode of continuously picking up still images (i.e., noted that the element IR is capable of continuously picking up still images; see col. 6, lines 50+), carry out in parallel a writing operation of writing an image (i.e., noted the parallel processing used for writing the image data in the first memory area 9261 and the second memory area 9262/9263; see col. 6, lines 25+, col. 8, lines 15+ and col. 9, lines 5+), obtained by said image pickup element (IR), into the first area (i.e., noted the area 9261 as shown in Fig. 3A) of said memory (IM/926) and a writing operation of writing the image, subjected to the predetermined signal processing by said signal processing circuit, into a second area of said memory (i.e., noted the writing operation of the compressed image into the memory area 9262, which is parallel to the writing of the image data into the memory area 9261; see Figs. 3A-7; see col. 8, lines 15-68 and col. 9, lines 5+).

Regarding claim 5, Yoshida '156 discloses wherein said signal processing circuit (i.e., the compressing circuit 928) and said memory control circuit (927) are included on a single integrated circuit (i.e., as shown in Figs. 1 and 2, the circuits 927 and 928 are integrated on the same single circuit unit IM).

Regarding claim 9, Yoshida '156 discloses a control method of an image pickup apparatus (i.e., Figs. 1 and 16) having an image pickup element (i.e. noted from Figs. 1 and 16, the Image Reader IR contain a sensor, such as CCD sensor, functioned as an image pickup element), a memory (i.e., the element 926 of Fig. 2) and a signal processing circuit (i.e., the element 928 of Fig. 2), said method comprising:

a first writing step of writing an image obtained by the image pickup element (i.e., the element IR), into a first area of the memory (i.e., noted that the image data provided by the image reader IR is writing into a first memory area 9261; see 3A-11; see col. 6, lines 25+, col. 8, lines 15+ and col. 9, lines 5+),

a reading step of reading the image already stored in the first area of the memory (i.e., noted from Figs. 3A-5, the image data already stored in the memory area 9261 is read out to the processing circuit 928 to perform a compressing process; see col. 6, lines 25+, col. 8, lines 15+ and col. 9, lines 5+);

a signal processing step for predetermined signal processing on the image read out of the first area of the memory by said reading step (i.e., noted that the processing circuit 928 is capable of processing the image data read out from the first memory area 9261; see col. 6, lines 25+, col. 8, lines 15+ and col. 9, lines 5+); and

a second writing step of writing the image subjected to the predetermined signal processing in said processing step into a second area of the memory (i.e., noted the compressed image data are writing into the second memory area 9262; see Figs. 3A-7; and col. 6, lines 25+, col. 8, lines 15+ and col. 9, lines 5+), wherein said second writing step is performed in parallel with said first writing step (i.e., noted the parallel processing of the image data writing process

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for the memory area 9261 and 9262 as discussed in col. 6, lines 25+, col. 8, lines 15+ and col. 9, lines 5+).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida '156 in view of Horii (U.S. 6,018,363).

Regarding claim 2, it is noted that although Yoshida '156 shown the use of signal processing unit (928) for performing compressing processing of the image data read out of the first area (9261) of the memory (926), Yoshida '156 does not explicitly shown the step of carrying out "white balance" processing are required by the present claimed invention.

However, the above-mentioned claimed limitations are well known in the art as evidenced by Horri '363. In particular, Horri 363 teaches the use of signal processing circuit (i.e., see the element 31 of Fig. 4; see col. 9, lines 15+) in the image pickup apparatus for carrying out white balance processing on the image data read out form the first memory element (4) so that the image quality can be enhanced.

In view of the above, having the system of Yoshida '156 and then given the well-established teaching of Horri '363, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the system of Yoshida '156 by providing a

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white balance processing function as taught by Horri '363 in order to improve the quality of the image captured by the image pickup element.

8. Claims 1 and 4 rejected under 35 U.S.C. 103(a) as being unpatentable over Kitagawa et al. (U.S. 6,738,093) in view of Yoshida '156.

Regarding claim 6, Kitagawa '093 discloses an image pickup apparatus comprising: an image pickup element (see Fig. 1, the element 1); a memory for storing an image obtained by the image pickup element (i.e., noted the memory 11);

an signal processing circuit (i.e., noted the element 4; col. 2, lines 60-68) adapted to effect predetermined signal processing (i.e., compress an image) on the image read out of the first area of said memory (11; noted that memory 11 contains a first area for storing a first frame of image data as shown in Figs. 4-6); and a memory control circuit (i.e., noted the element 5 of Fig. 1) adapted to, in a mode of continuously pickup still image (i.e., see Figs. 4, 5 and 6; col. 3, lines 5+ and col. 5, lines 25-30), carry out in parallel a writing operation (i.e., noted WRITE operation as shown in Figs. 4, 5 and 6) of writing an image obtained by said image pickup element (1), into the first area of said memory (11) (11; noted that memory 11 contains a first area for storing a first frame of image data as shown in Figs. 4-6) and a readout operation (i.e., noted the "READ" operation parallel to "WRITE" operation as shown in Figs. 4-6) of reading an image already stored in the first area of the said memory (11) to be compressed by the image compressing circuit (i.e., as shown in Fig. 4, the first frame stored in the first area of the memory 11 is read and compressed by the processing section 4; see Figs. 4-6).

Moreover, it is noted that Kitagawa '093 does not explicitly shown the use of the memory having a second memory area for writing the processed images and writing of the image data in the first memory area and the second memory area of the memory is performed in parallel to each other as recited in present claimed invention.

However, the above-mentioned claimed limitations are well known in the art as evidenced by Yoshida '156. In particular, Yoshida '156 teaches the use of a memory element (i.e., the memory 926 of Fig. 2) and a signal processing circuit (928) and a memory control circuit (927) for writing the image data, captured by the image pickup element (IR), into a first area (9261) of the memory (926) which is performed in parallel with writing the image data, subject to be compression processing by the signal processing circuit, into a second area (9262) of the memory (926) (i.e., noted the writing operation of the compressed image into the memory area 9262, which is parallel to the writing of the image data into the memory area 9261; see Figs. 3A-7; see col. 8, lines 15-68 and col. 9, lines 5+) so that the entire processing/writing time for the image data can be reduced owing to the parallel processing (i.e., see col. 9, lines 10+).

In view of the above, having the system of Kitagawa '093 and then given the well-established teaching of Yoshida '156, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the memory circuit of Kitagawa '093 as taught by Yoshida '156, since Yoshida '156 suggested in col. 9, lines 10+ that such a modification would reduce the entire processing/writing time for the image data in the image pickup apparatus.

Regarding claim 4, the combination of Kitagawa '093 and Yoshida '156 discloses wherein said memory control circuit (i.e., the circuit 5 of Kitagawa '093; and the circuit 927 of

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Yoshida '156) further carries out a read operation of reading the image stored in a second area of said memory (i.e., noted reading of the second frame at the time t15-t16 which stored in the memory 11 during the time T12-T13 as shown in Kitagawa '093; and noted the reading of image data from the second memory area 9262 by the control circuit 927) in parallel with the writing operation and the readout operation (i.e., noted the "WRITE" and "READ" operation as shown in Figs. 4-6 of Kitagawa '093; and noted the writing/reading of the image data form the memory areas 9261, 9262 and 9263 are performed in parallel by using parallel processing, see col. 8, lines 15-68 and col. 9, lines 5+), to record the image in a recording medium (i.e., noted the recording medium 7).

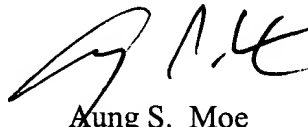
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aung S. Moe whose telephone number is 571-272-7314. The examiner can normally be reached on Flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward F. Urban can be reached on 571-272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Aung S. Moe
Primary Examiner
Art Unit 2685

A. Moe
August 9, 2005